

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yuri Mirgorodski et al.

Application No.: 10/664,469

Filed: September 17, 2003

For: METHOD OF PMOS STACKED-

GATE MEMORY CELL

PROGRAMMING ENHANCEMENT UTILIZING STAIR-LIKE PULSES OF CONTROL GATE VOLTAGE Group No.: 2818

Examiner: Unknown

SUBMISSION OF POWER OF ATTORNEY BY ASSIGNEE

353 Sacramento Street, Suite 2200 San Francisco, CA 94111 Telephone: (415) 772-4900 Facsimile: (415) 398-2890

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Enclosed for filing please find a duly executed Power of Attorney by Assignee for the above-identified application which specifies an Assignment recordal date of <u>January 15, 2004</u>, at Reel <u>014884</u>, Frame <u>0437</u>, and shows Assignee's entire right, title and interest to establish ownership.

Respectfully submitted,

STALLMAN & POLLOCK LLP

Date: August 31, 2004

Michael J. Pollock (Reg. No. 29,098)

Attorneys for Applicant(s)

Atty Docket No.: NSC1-M3500 [P05681]



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VOLTAGE

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

NATIONAL SEMICONDUCTOR CORPORATION, assignee of the entire right title and interest in the above-identified application by assignment dated January 8, 2004, which assignment was recorded in the Patent and Trademark Office on January 15, 2004, at Reel 014884, Frame 0437, hereby appoints the members of the firm of STALLMAN & POLLOCK LLP, a firm composed of:

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as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

Please direct all correspondence regarding this application to the following:

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Name: Title:

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Atty Docket No.: NSC1- M3500 [P05681]